

FIG. 1 is a schematic diagram of a display frame 10, showing a grid of pixels 30. The grid is composed of 20 columns and 10 rows of pixels. A single pixel is labeled 30.

pixel 30

display frame 10

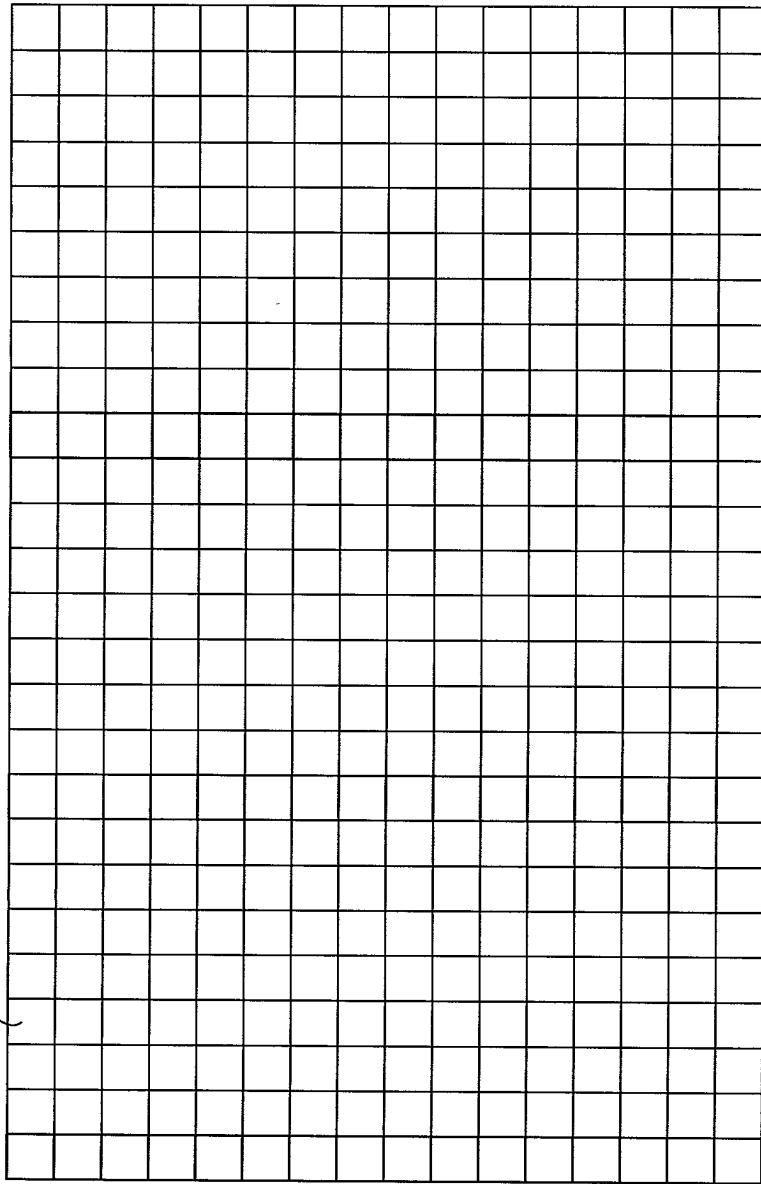


FIG. 1

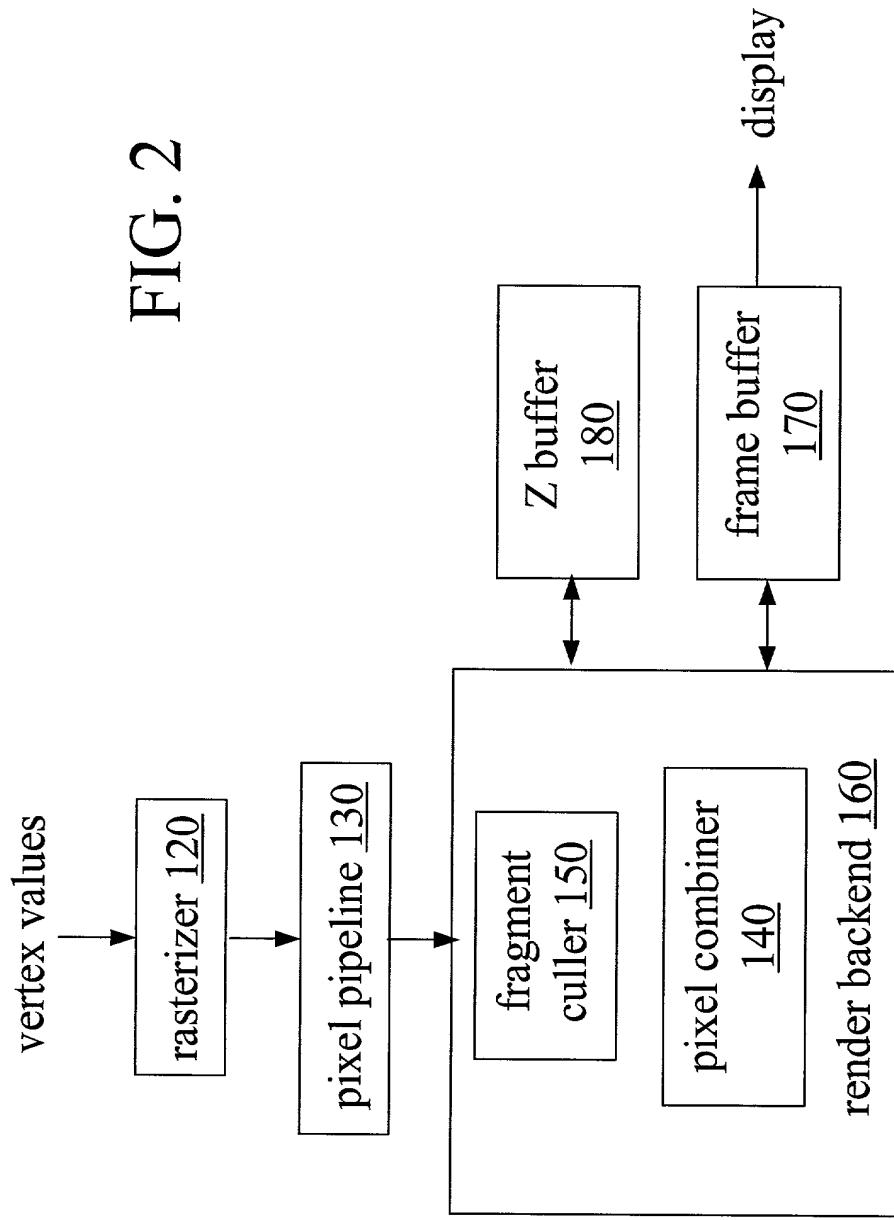


FIG. 2

FIG. 3 is a block diagram of a graphics pipeline. The pipeline starts with vertex values, which are processed by a transform and lighting engine 110. The output of the engine 110 is then processed by a rasterizer 120. The output of the rasterizer 120 is then processed by a pixel pipeline 130. The output of the pixel pipeline 130 is then processed by a fragment culler 150 and a pixel combiner 140. The output of the pixel combiner 140 is then processed by a Z buffer 180 and a frame buffer 170. The output of the frame buffer 170 is then displayed on a display.

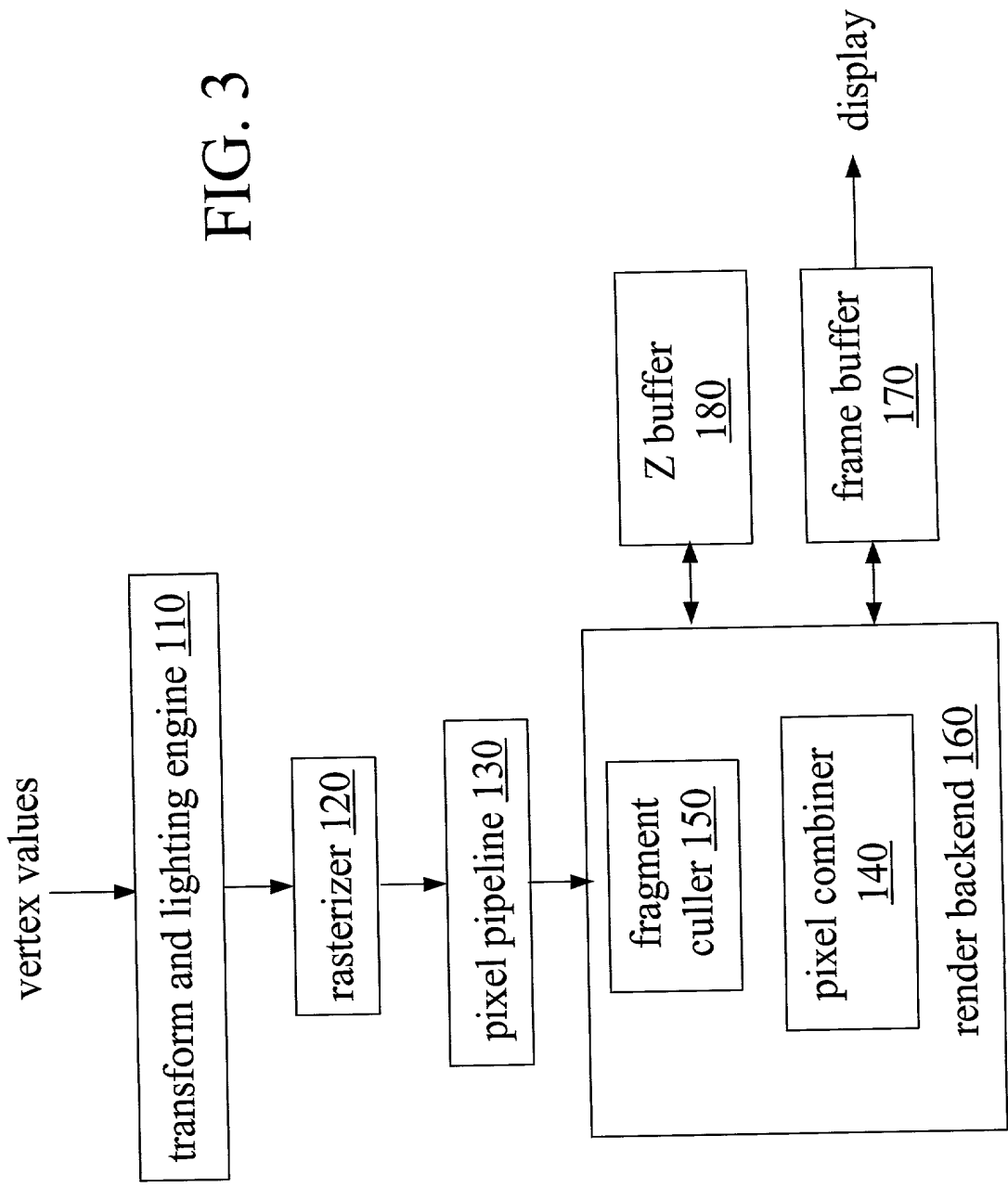


FIG. 3

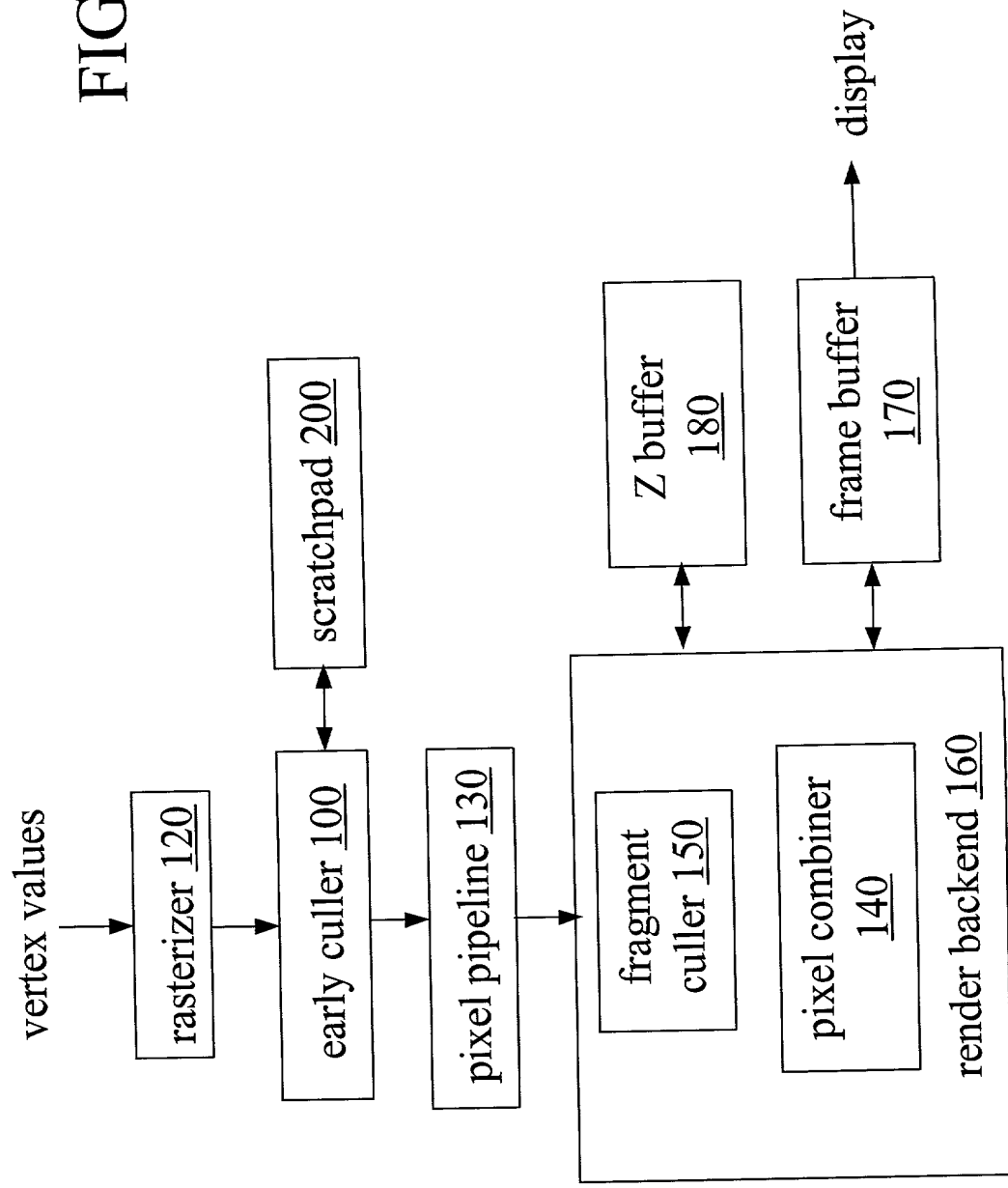


FIG. 4

FIG. 5 is a schematic diagram of a display frame 10. The display frame 10 is divided into a grid of pixel blocks 20. A single pixel block 20 is further divided into a grid of pixels 30. The diagram illustrates the hierarchical structure of the display frame, showing how it is composed of multiple pixel blocks, which in turn are composed of individual pixels.

display
frame 10

pixel
block 20

pixel
30

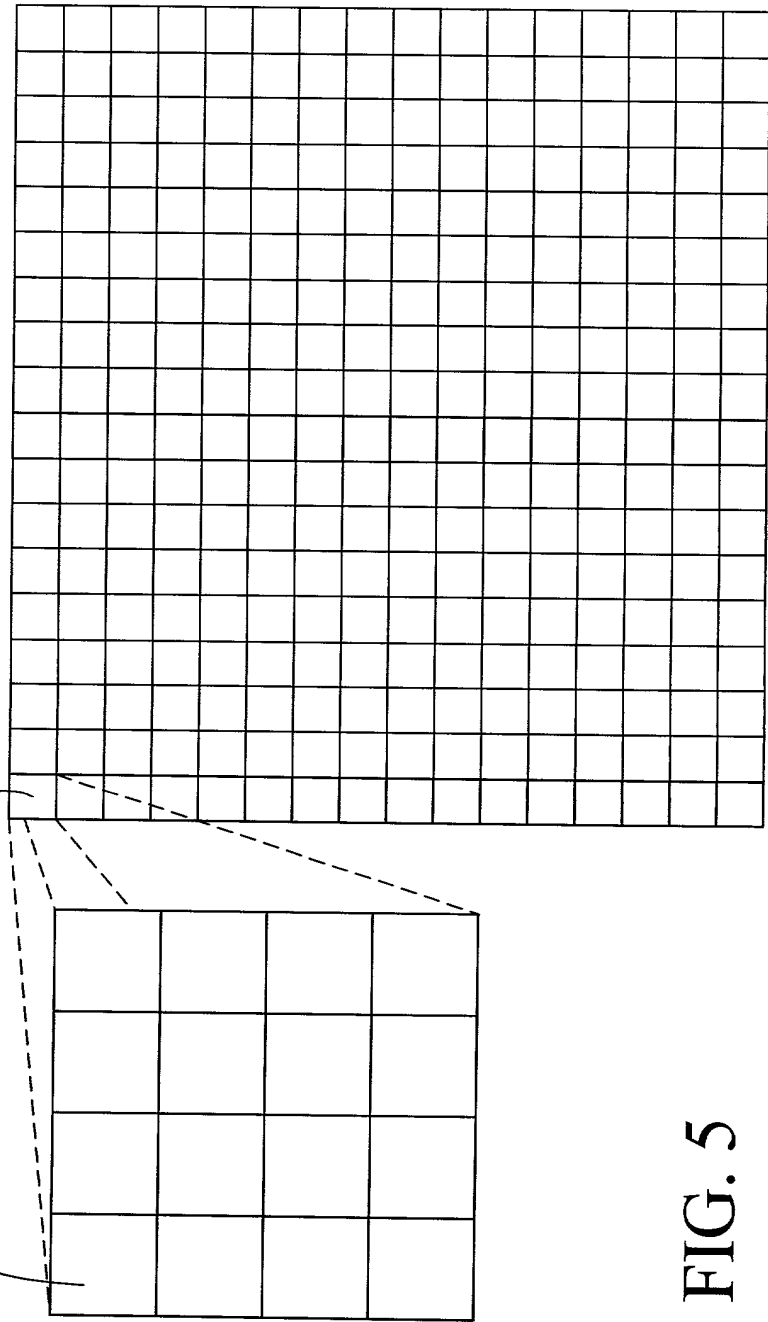


FIG. 5

FIG. 6

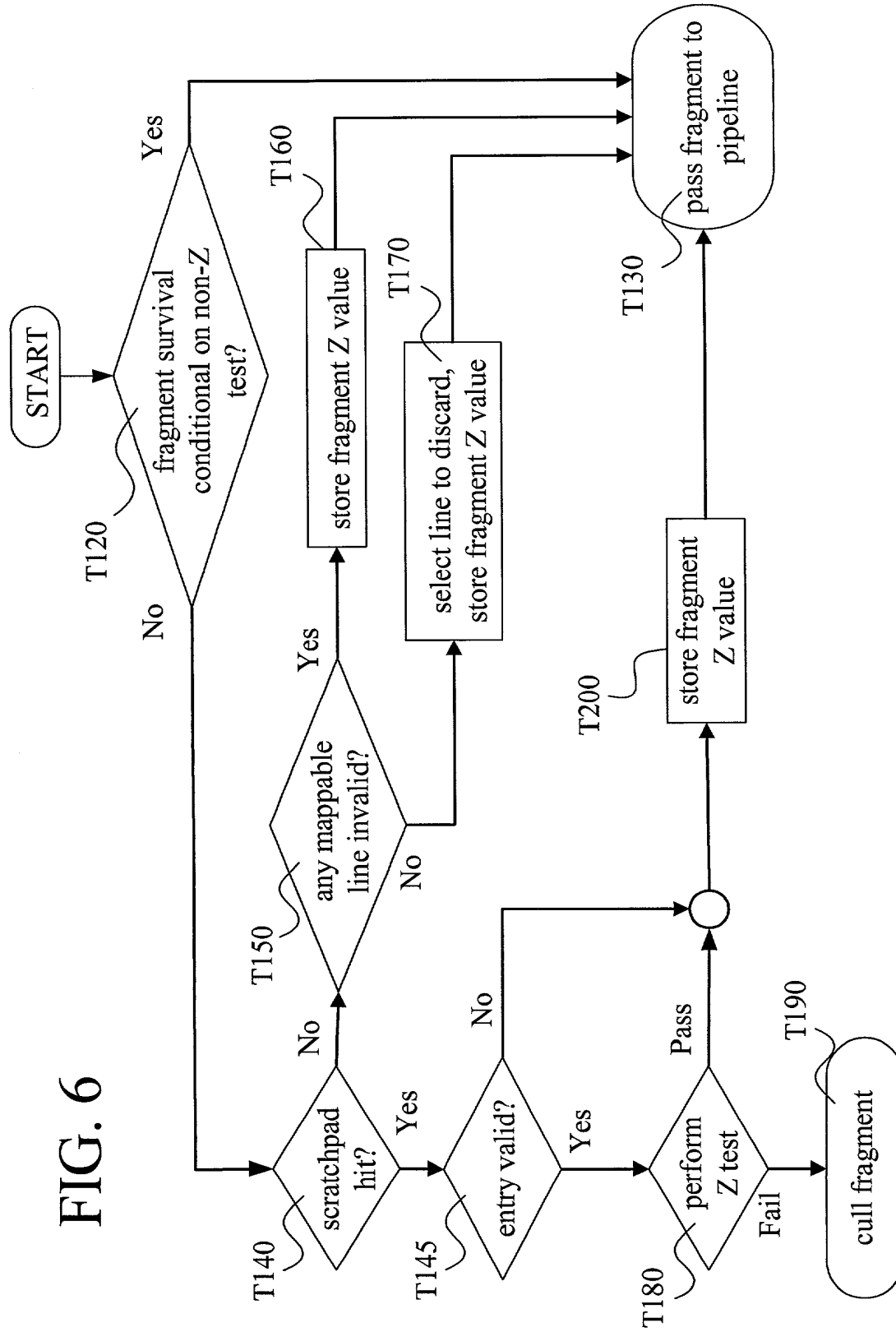
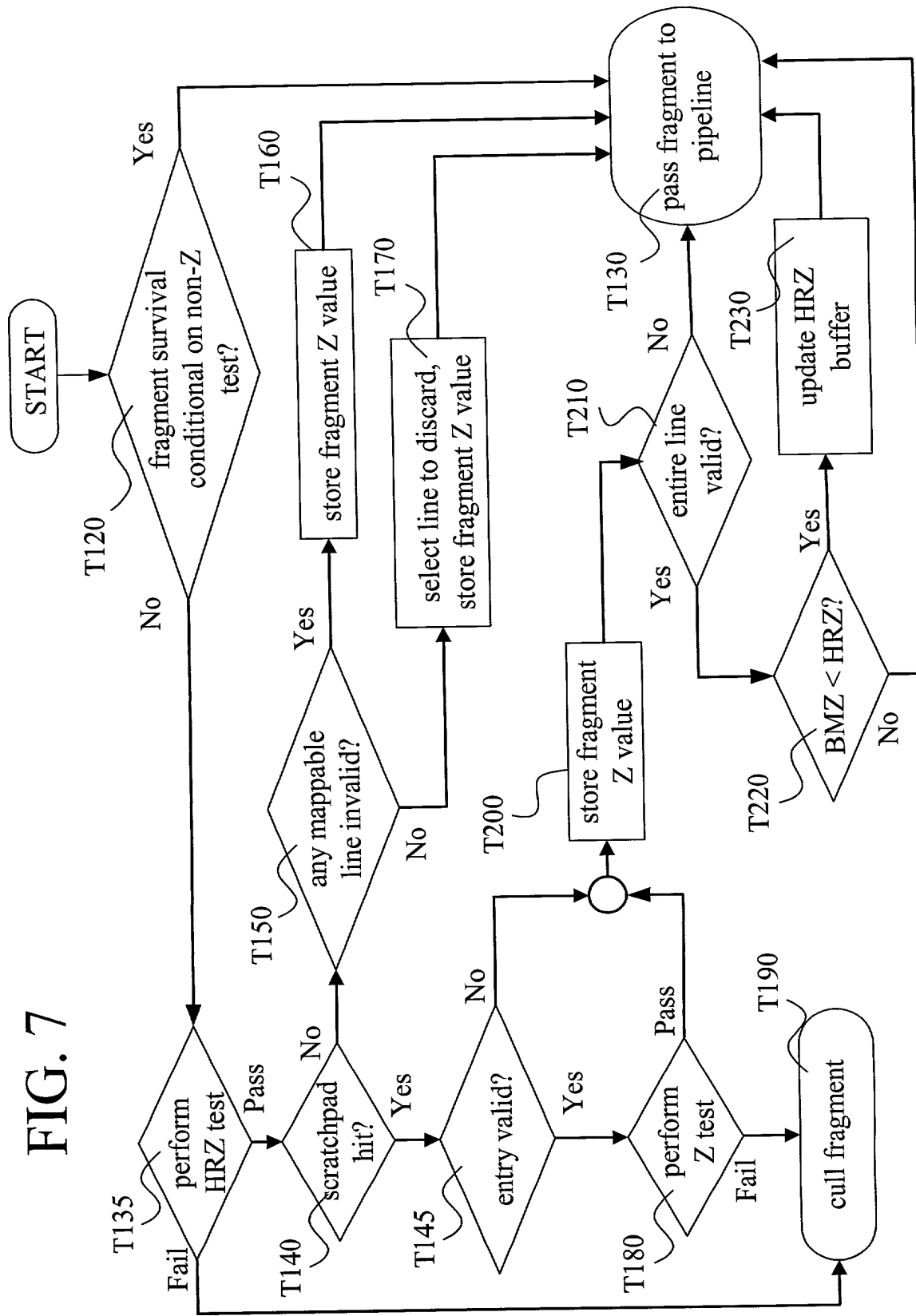


FIG. 7



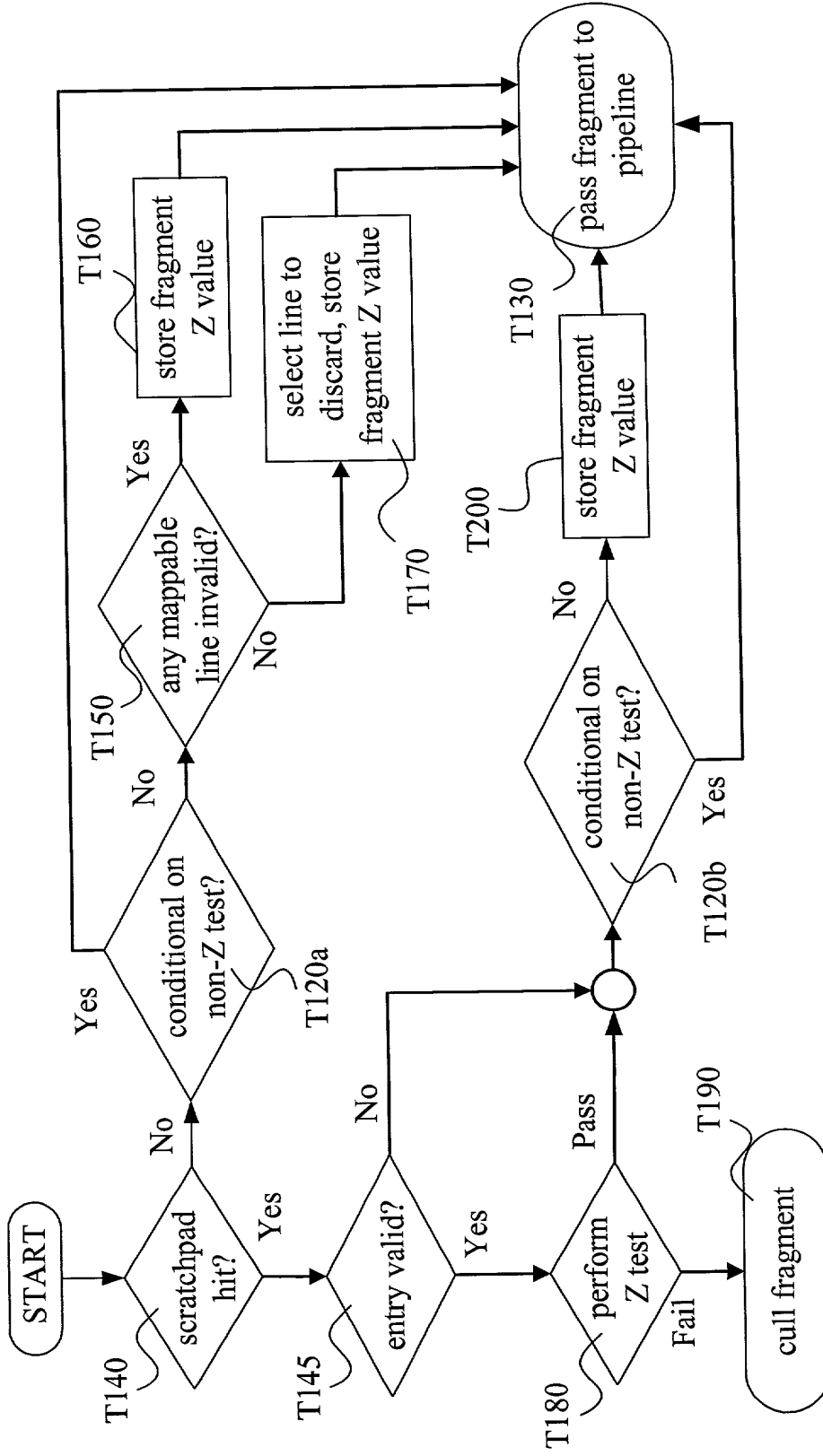


FIG. 8

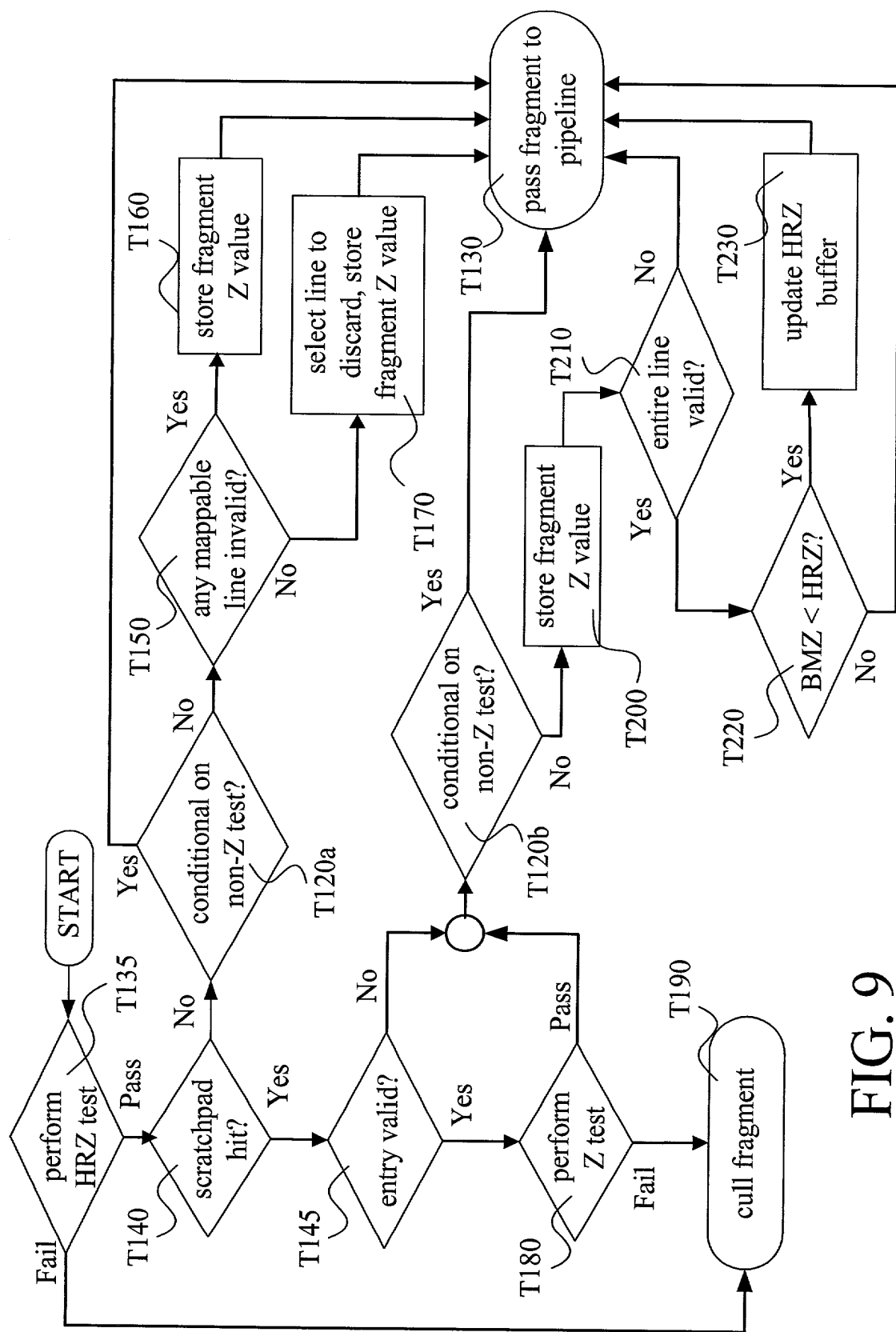


FIG. 9

FIG. 10

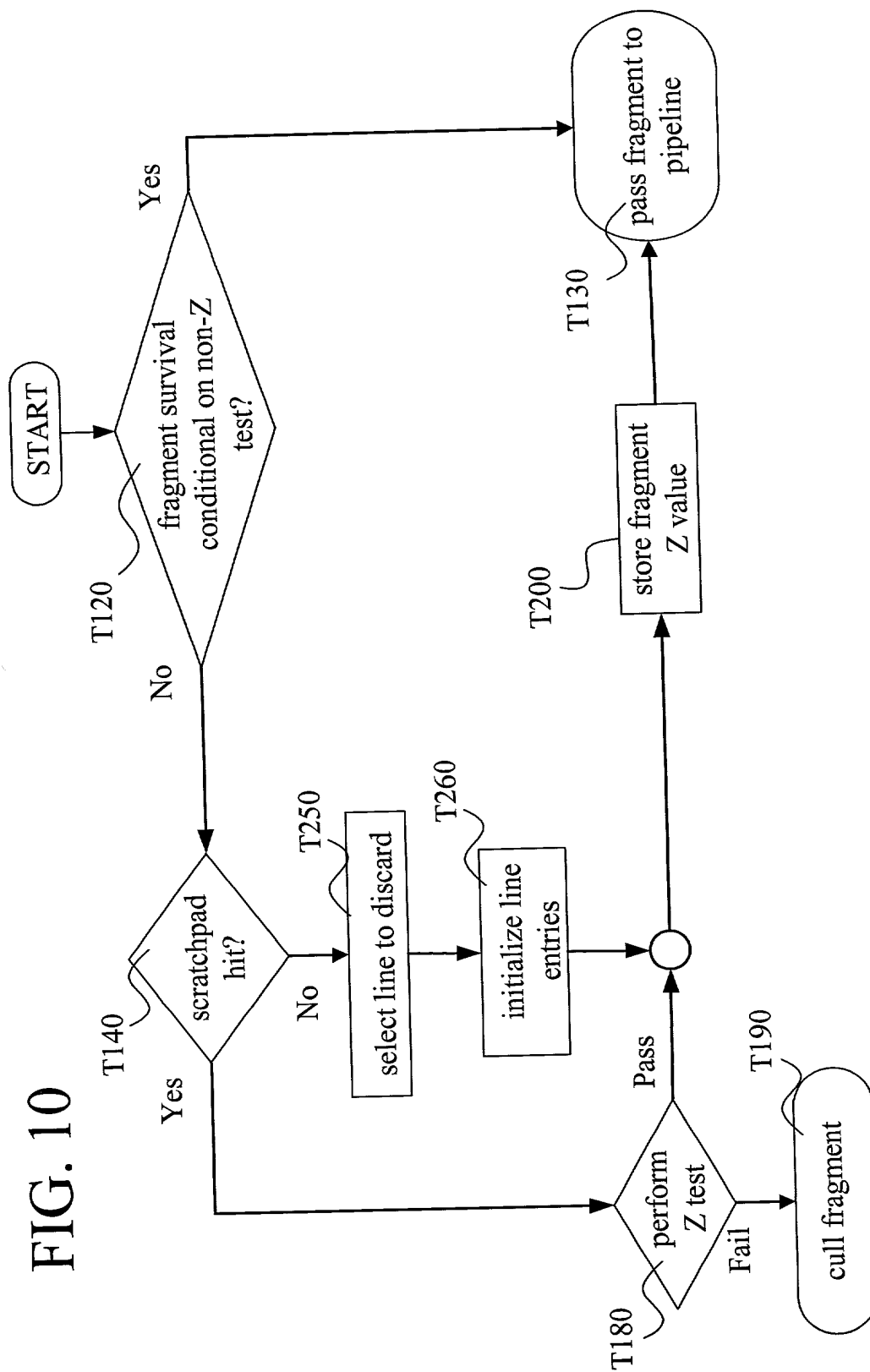


FIG. 11

FIG. 11

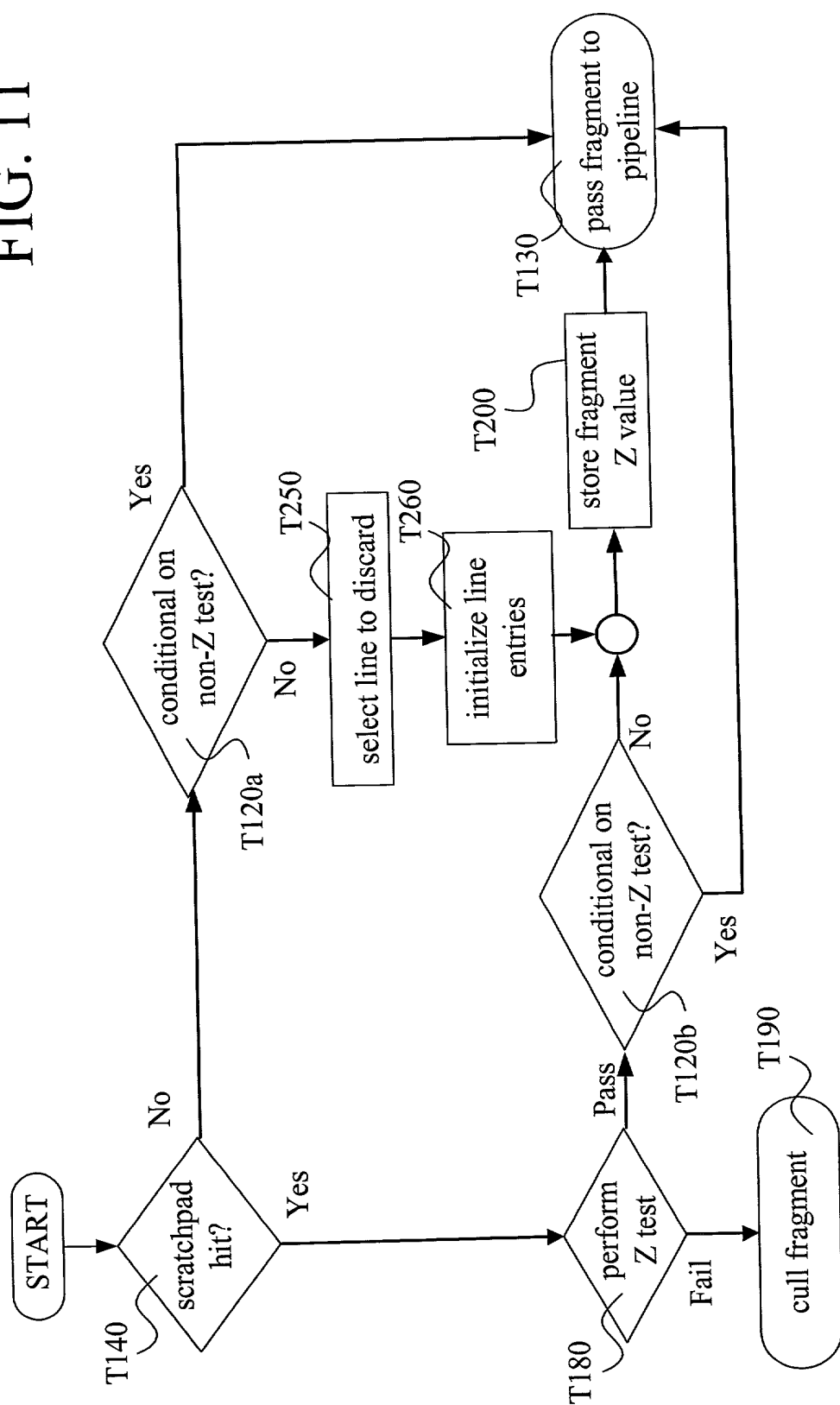


FIG. 12

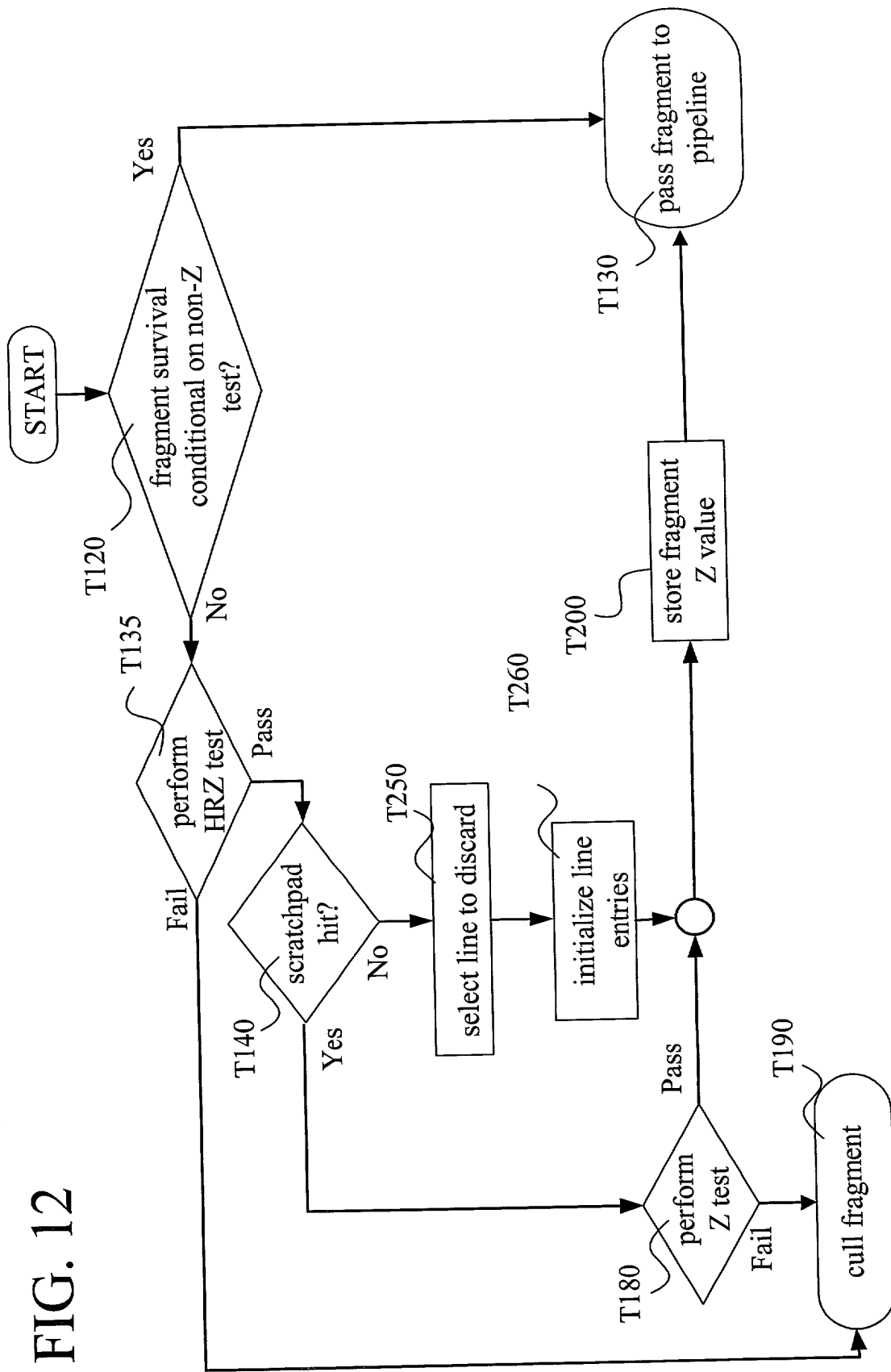


FIG. 13

